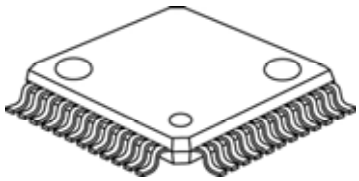
3x8-channel Constant Current LED Driver with Compulsory Open-Circuit Detection

Features

- 24 constant-current output channels
  - Output channels of 3 groups are interleavingly arranged
  - 3 $\overline{OE}$ control each group individually
- Constant output current range per channel: 1~35mA
  - 1~35mA @ 5V supply voltage
  - 1~25mA @ 3.3V supply voltage
  - In 3 different color groups, each group is set by an external resistor
- Excellent output current accuracy,
  - Between different groups from $\overline{OUTA0}$ ~ $\overline{OUTA7}$, $\overline{OUTB0}$ ~ $\overline{OUTB7}$, and $\overline{OUTC0}$ ~ $\overline{OUTC7}$ of channels: <±2% (typ.), and
  - Between different groups from $\overline{OUTA0}$ ~ $\overline{OUTA7}$, $\overline{OUTB0}$ ~ $\overline{OUTB7}$, and $\overline{OUTC0}$ ~ $\overline{OUTC7}$ of ICs: <±4% (typ.)
- Fast response of output current
  - Min. output pulse width of $\overline{OE}$: 70ns
- Compulsory open-circuit detection
  - Open-circuit LEDs can be detected
  - Full panel, data independent
  - Flicker-free error detection with small energy
- Staggered delay of output, preventing from current surge
- 25MHz clock frequency
- Schmitt trigger input

LQFP



GLQ: LQFP48L-7x7-0.5

Product Description

MBI5324 is an enhanced 3x8-channel constant current LED sink driver with smart error detection. The output ports are arranged in three groups and each group is set by an external resistor for one color. Users may adjust the output current from 1mA to 35mA with three external resistors R-EXTA, R-EXTB, R-EXTC, which provide users flexibility in controlling the light intensity and white balance of LEDs. The output current of 1mA is designed for small current applications.

Moreover, there are three $\overline{OE}$ controlling each output group individually. It has the same control scheme as MBI5026 to facilitate white balance.

The output channels of 3 groups are interleavingly arranged in $\overline{OUTA0}$-$\overline{OUTB0}$-$\overline{OUTC0}$, $\overline{OUTA1}$-$\overline{OUTB1}$-$\overline{OUTC1}$…$\overline{OUTA7}$-$\overline{OUTB7}$-$\overline{OUTC7}$. The arrangement helps PCB layout easy to design. It's very useful for fine-pitch LED displays, LED mesh displays or LED strips applications.

MBI5324 contains a 24-bit shift register and a 24-bit output latch, which convert serial input data into parallel output format. At MBI5324 output stages, 24 regulated current ports are designed to provide uniform and constant current sinks with small skew between ports for driving LEDs within a wide range of forward voltage (V_F) variations.

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MBI5324 guarantees to endure maximum 17V at the output ports. Besides, the high clock frequency with up to 25MHz also satisfies the system requirements for high volume data transmission.

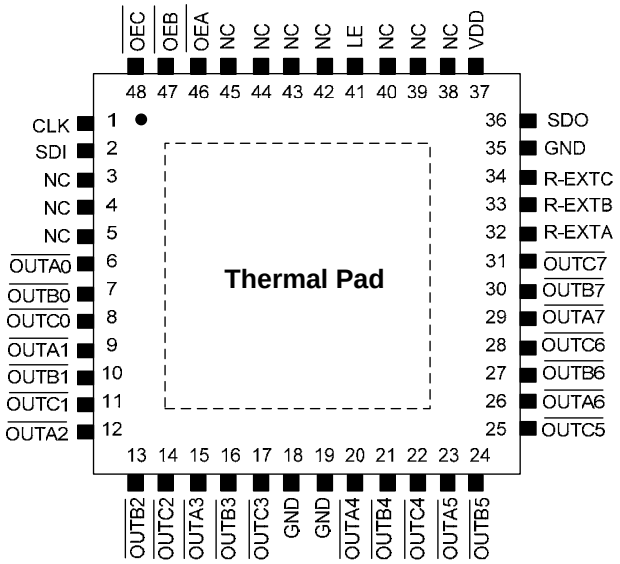
MBI5324 provides compulsory open-circuit detection. With the open-circuit detection, MBI5324 can detect individual LED open-circuit error without extra components. Once the dedicated command is issued, all of the output ports will be turned on with small current. Since the turn-on duration and current are so small, the flicker will not be sensed by human eyes and the image quality will not be impacted. All of the channels are detected no matter the input data is zero or one.

MBI5324 exploits **PrecisionDrive™** technology to enhance the output characteristics. The control method is similar to the conventional 16-channel LED driver IC, e.g. MBI5026 and MBI5039. Users can use the same controller hardware and simply rearrange the RGB data sequence to control MBI5324.

Applications

- Fine-pitch LED video displays
- LED mesh displays
- LED strips

Pin Configuration



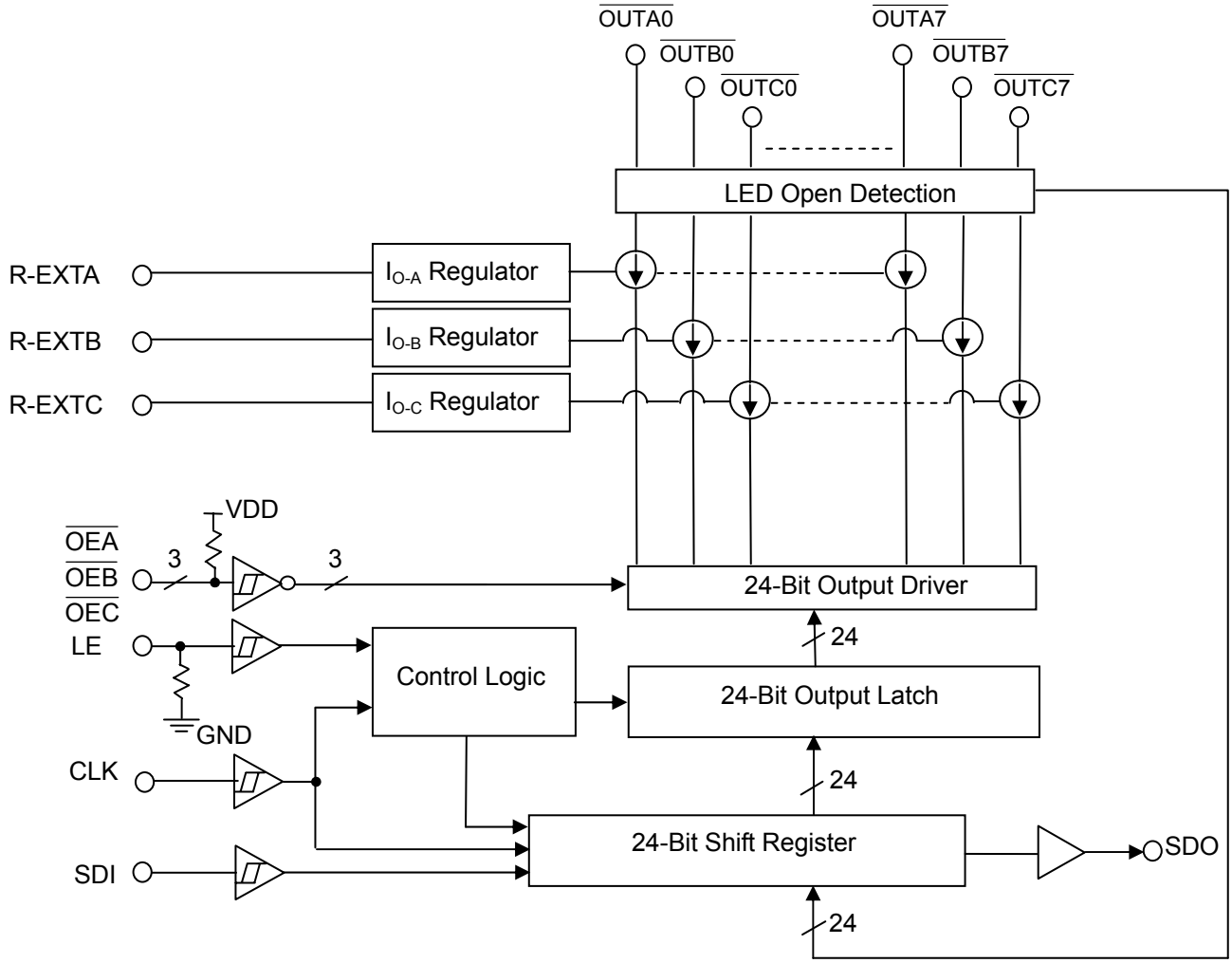
MBI5324GLQ
Top View

Terminal Description

Pin	Pin Name	Description and Function
18,19,35	GND	Ground terminal for control logic and current sinks
2	SDI	Serial-data input to the shift register
1	CLK	Clock input terminal used to shift data on rising edge and to carry command information when LE is asserted.
41	LE	Data strobe terminal to assert command with adequate CLK pulses
6,9,12,15, 20,23,26,29	$\overline{OUTA0}$ ~ $\overline{OUTA7}$	Constant current output terminals of “A” group
7,10,13,16,21, 24,27,30	$\overline{OUTB0}$ ~ $\overline{OUTB7}$	Constant current output terminals of “B” group
8,11,14,17,22 25,28,31	$\overline{OUTC0}$ ~ $\overline{OUTC7}$	Constant current output terminals of “C” group
46,47,48	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$	Enable “A”, “B”, and “C” output drivers to sink current. When its level is low (active), the output drivers are enabled; otherwise, the output drivers are turned OFF (blank).
36	SDO	Serial-data output to the SDI of the following driver IC
32~34	R-EXTA, B, C	Input terminal used for connecting an external resistor in order to set up the current level of all “A”, “B”, and “C” output ports
37	VDD	3.3/5V supply voltage terminal
-	Thermal Pad	Heat dissipation pad.* Please connect to GND.

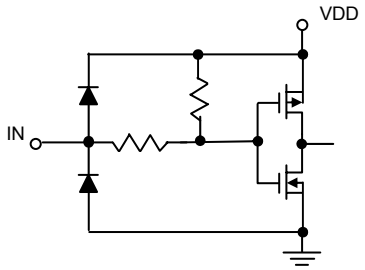
*The desired thermal conductivity will be improved on condition that a heat-conducting copper foil on PCB is soldered with a thermal pad.

Block Diagram

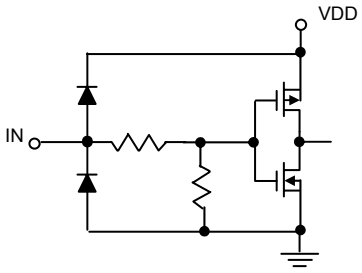


Equivalent Circuits of Inputs and Outputs

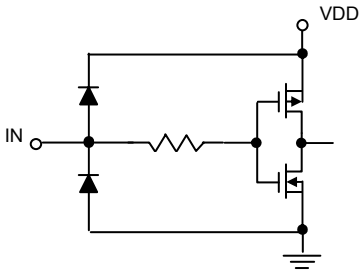
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$, $\overline{\text{OEC}}$ terminal



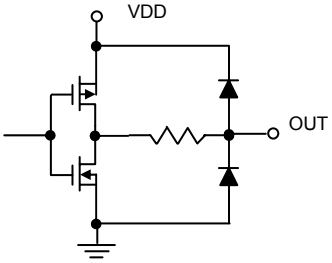
LE terminal



CLK, SDI terminal



SDO terminal



Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Input Pin Voltage (SDI, $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$, LE, CLK)		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	35	mA
Sustaining Voltage at $\overline{OUTn}$ Pins		V_{DS}	-0.5~17	V
GND Terminal Current		I_{GND}	840	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GLQ Type	P_D	2.37	W
Thermal Resistance (On 4 Layer PCB, Ta=25°C)*	GLQ Type	$R_{th(j-a)}$	52.6	°C/W
Operating Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM (MIL-STD-883G Method 3015.7, Human Body Mode)	-	Class 3A (4000V~7999V)	-
	MM (JEDEC EIA/JESD22-A115, Machine Mode)	-	Class B (200V~399V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTA0}$ ~ $\overline{OUTC7}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		1	-	35	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta= -40~85ºC		0.75xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta= -40~85ºC		GND	-	0.27xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}= 17.0V and channel off		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)*		dI_{OUT1}	I_{OUT}= 20mA V_{DS}= 1.0V	R_{ext}= 700Ω	-	±2.0	±4.0	%
Current Skew (IC)**		dI_{OUT2}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}= 700Ω	-	±4.0	±6.0	%
Output Current vs. Output Voltage Regulation***		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}= 700Ω@20mA		-	±1	±2	% / V
Output Current vs. Supply Voltage Regulation***		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±0.5	±1.0	% / V
Open-Circuit Detection Threshold Voltage****		$V_{OD,TH}$	-		-	0.3	-	V
Pull-up Resistor		R_{IN}(up)	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$		250	500	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE		250	500	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUTA0}$ ~ $\overline{OUTC7}$=Off		-	4.4	-	mA
		I_{DD}(off) 2	R_{ext}=700Ω, $\overline{OUTA0}$ ~ $\overline{OUTC7}$=Off		-	12.0	-	
	"On"	I_{DD}(on) 1	R_{ext}=700Ω, $\overline{OUTA0}$ ~ $\overline{OUTC7}$=Off		-	13.0	-	

* Current skew (channel) can be divided into different groups from $\overline{OUTA0}$ ~ $\overline{OUTA7}$, $\overline{OUTB0}$ ~ $\overline{OUTB7}$, and $\overline{OUTC0}$ ~ $\overline{OUTC7}$).

**Current skew (IC) refers to same channel current between different groups from $\overline{OUTA0}$ ~ $\overline{OUTA7}$, $\overline{OUTB0}$ ~ $\overline{OUTB7}$, and $\overline{OUTC0}$ ~ $\overline{OUTC7}$) of different ICs.

***One channel on.

****Open-circuit detection threshold voltage ($V_{OD,TH}$) is a configurable voltage.

Electrical Characteristics (V_{DD}=3.3V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	All OUT ports		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		1	-	25	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta= -40~85ºC		0.75xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta= -40~85ºC		GND	-	0.27xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}= 17.0V and channel off		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}= -1.0mA		2.9	-	-	V
Current Skew (Channel)*		dI_{OUT1}	I_{OUT}= 20mA V_{DS}= 1.0V	R_{ext}=700Ω	-	±2	±4.0	%
Current Skew (IC)**		dI_{OUT2}	I_{OUT}= 20mA V_{DS}= 1.0V	R_{ext}=700Ω	-	±4	±6.0	%
Output Current vs. Output Voltage Regulation***		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}= 700Ω@20mA		-	±1	±2	% / V
Output Current vs. Supply Voltage Regulation***		$\%/dV_{DD}$	V_{DD} within 3.0V and 3.6V		-	±0.5	±1.0	% / V
Open-Circuit Detection Threshold Voltage****		$V_{OD,TH}$	-		-	0.3	-	V
Pull-up Resistor		R_{IN}(up)	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$		250	500	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE		250	500	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUTA0}$ ~ $\overline{OUTC7}$=Off		-	4.0	-	mA
		I_{DD}(off) 2	R_{ext}=700Ω, $\overline{OUTA0}$ ~ $\overline{OUTC7}$=Off		-	11.6	-	
	"On"	I_{DD}(on) 1	R_{ext}=700Ω, $\overline{OUTA0}$ ~ $\overline{OUTC7}$=Off		-	12.0	-	

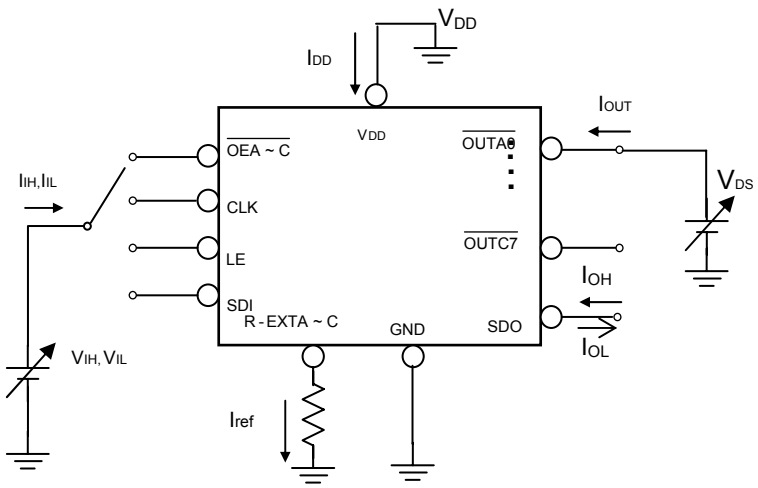
* Current skew (channel) can be divided into different groups from $\overline{OUTA0}$ ~ $\overline{OUTA7}$, $\overline{OUTB0}$ ~ $\overline{OUTB7}$, and $\overline{OUTC0}$ ~ $\overline{OUTC7}$).

**Current skew (IC) refers to same channel current between different groups from $\overline{OUTA0}$ ~ $\overline{OUTA7}$, $\overline{OUTB0}$ ~ $\overline{OUTB7}$, and $\overline{OUTC0}$ ~ $\overline{OUTC7}$) of different ICs.

***One channel on.

****Open-circuit detection threshold voltage ($V_{OD,TH}$) is a configurable voltage.

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}=5.0V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	LE-SDO	t_{pLS}	V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω R_L=162Ω C_L=10pF I_{OUT}=20mA C_1=100nF C_2=22μF C_{SDO}=10pF	-	55	70	ns
	CLK-SDO	t_{pLH1}		-	35	40	ns
	LE-$\overline{OUTA0}$	t_{pLH2}		-	35	-	ns
	$\overline{OE}$ - $\overline{OUTA0}$	t_{pLH3}		-	40	-	ns
Propagation Delay Time ("H" to "L")	LE-SDO	t_{pLS}		-	55	70	ns
	CLK-SDO	t_{pHL1}		-	25	30	ns
	LE-$\overline{OUTA0}$	t_{pHL2}		-	50	-	ns
	$\overline{OE}$ - $\overline{OUTA0}$	t_{pHL3}		-	55	-	ns
Staggered Delay of Output	$\overline{OUTAn}$ - $\overline{OUTAn+1}$ $\overline{OUTBn}$ - $\overline{OUTBn+1}$ $\overline{OUTCn}$ - $\overline{OUTCn+1}$	t_{stag}		-	6	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		15	-	-	ns
	LE	$t_{w(L)}$		15	-	-	ns
Data Clock Frequency		F_{CLK}		-	-	25	MHz
Hold Time for LE		$t_{h(L)}$		10	-	-	ns
Setup Time for LE		$t_{su(L)}$		10	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
Maximum CLK Rise Time*		t_r		-	-	500	ns
Maximum CLK Fall Time*		t_f		-	-	500	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$t_{f,SDO}$		-	10	-	ns
Output Rise Time of Output Ports		t_{or}			35		ns
Output Fall Time of Output Ports		t_{of}		-	35	-	ns
Compulsory Error Detection Operation Time**		t_{ERR-C}		600	650	700	ns
$\overline{OE}$ Pulse Width***		$t_{w(OE)}$		-	70	-	ns

* If t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded drivers.

** The detection time of compulsory error detection is 600ns. However, it takes extra operation time to enter or exit the error detection mode. The specifications here list the total operation time for detection. Please refer to the section of principle of operation for details.

*** $\overline{OE}$ =t_{or}+t_{of}.

Switching Characteristics (V_{DD}=3.3V)

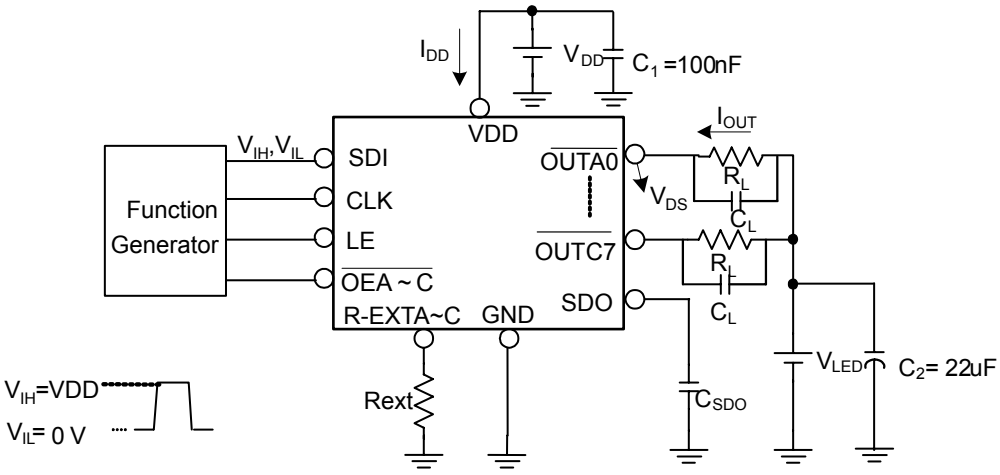
Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time (“L” to “H”)	LE-SDO	t_{pLS}	V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=700Ω R_L=162Ω C_L=10pF I_{OUT}=20mA C_1=100nF C_2=22μF C_{SDO}=10pF	-	85	100	ns
	CLK-SDO	t_{pLH1}		-	40	45	ns
	LE-$\overline{OUTA0}$	t_{pLH2}			50	-	ns
	$\overline{OE}$ -$\overline{OUTA0}$	t_{pLH3}		-	60	-	ns
Propagation Delay Time (“H” to “L”)	LE-SDO	t_{pLS}		-	85	100	ns
	CLK-SDO	t_{pHL1}		-	30	35	ns
	LE-$\overline{OUTA0}$	t_{pHL2}		-	55	-	ns
	$\overline{OE}$ -$\overline{OUTA0}$	t_{pHL3}		-	65	-	ns
Staggered Delay of Output	$\overline{OUTAn}$-$\overline{OUTAn+1}$ $\overline{OUTBn}$-$\overline{OUTBn+1}$ $\overline{OUTCn}$-$\overline{OUTCn+1}$	t_{stag}		-	8	-	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		15	-	-	ns
Data Clock Frequency		F_{CLK}		-	-	20	MHz
Hold Time for LE		$t_{h(L)}$		10	-	-	ns
Setup Time for LE		$t_{su(L)}$		10	-	-	ns
Hold Time for SDI		$t_{h(D)}$		5	-	-	ns
Setup Time for SDI		$t_{su(D)}$		3	-	-	ns
Maximum CLK Rise Time*		t_r		-	-	500	ns
Maximum CLK Fall Time*		t_f		-	-	500	ns
SDO Rise Time		$t_{r,SDO}$		-	10	-	ns
SDO Fall Time		$t_{f,SDO}$		-	10	-	ns
Output Rise Time of Output Ports		t_{or}			50		ns
Output Fall Time of Output Ports		t_{of}		-	50	-	ns
Compulsory Error Detection Operation Time **		t_{ERR-C}		600	650	700	ns
$\overline{OE}$ Pulse Width***		$t_{w(OE)}$		-	100	-	ns

*If t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded drivers.

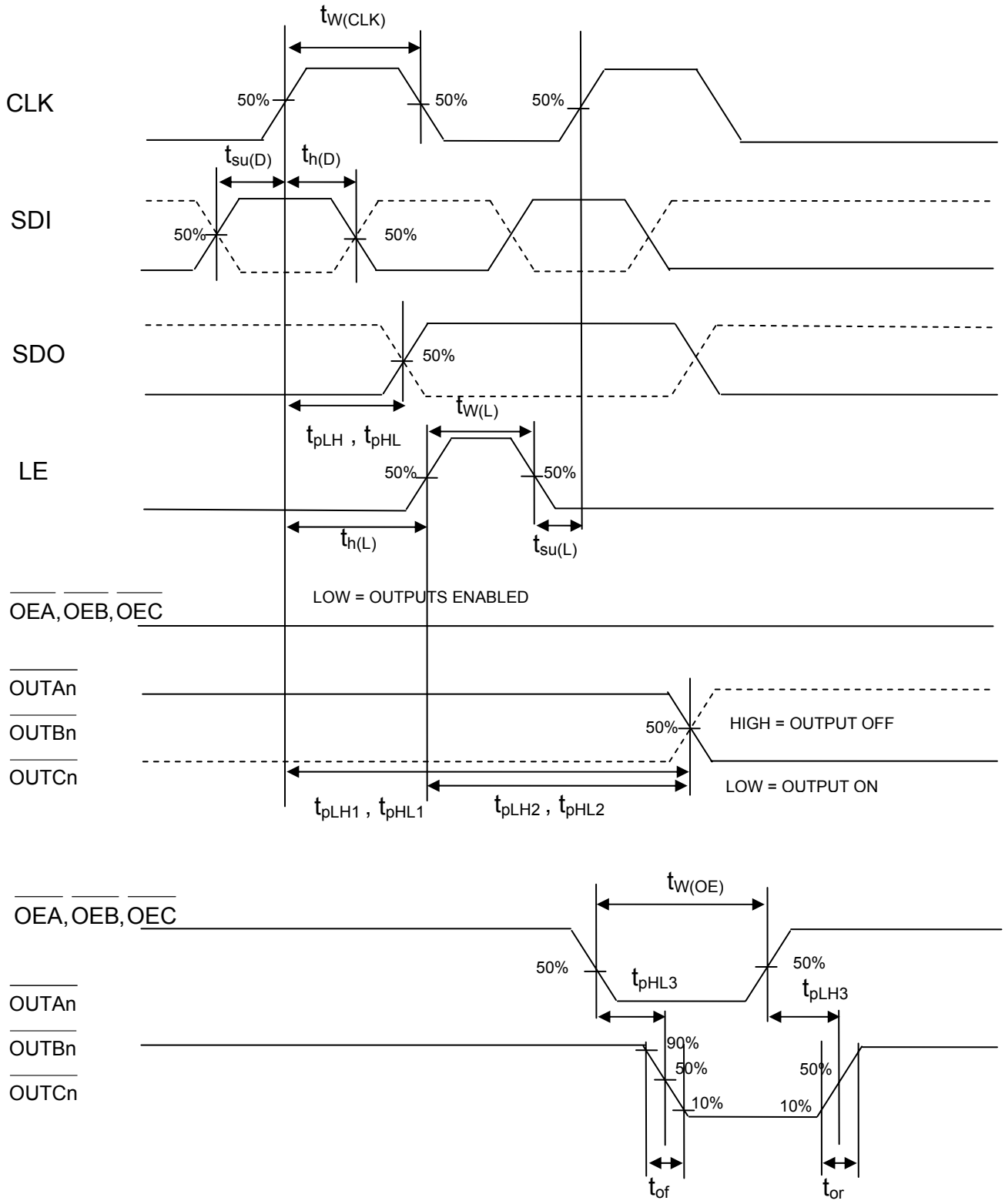
** The detection time of compulsory error detection is 600ns. However, it takes extra operation time to enter or exit the error detection mode. The specifications here list the total operation time for detection. Please refer to the section of principle of operation for details.

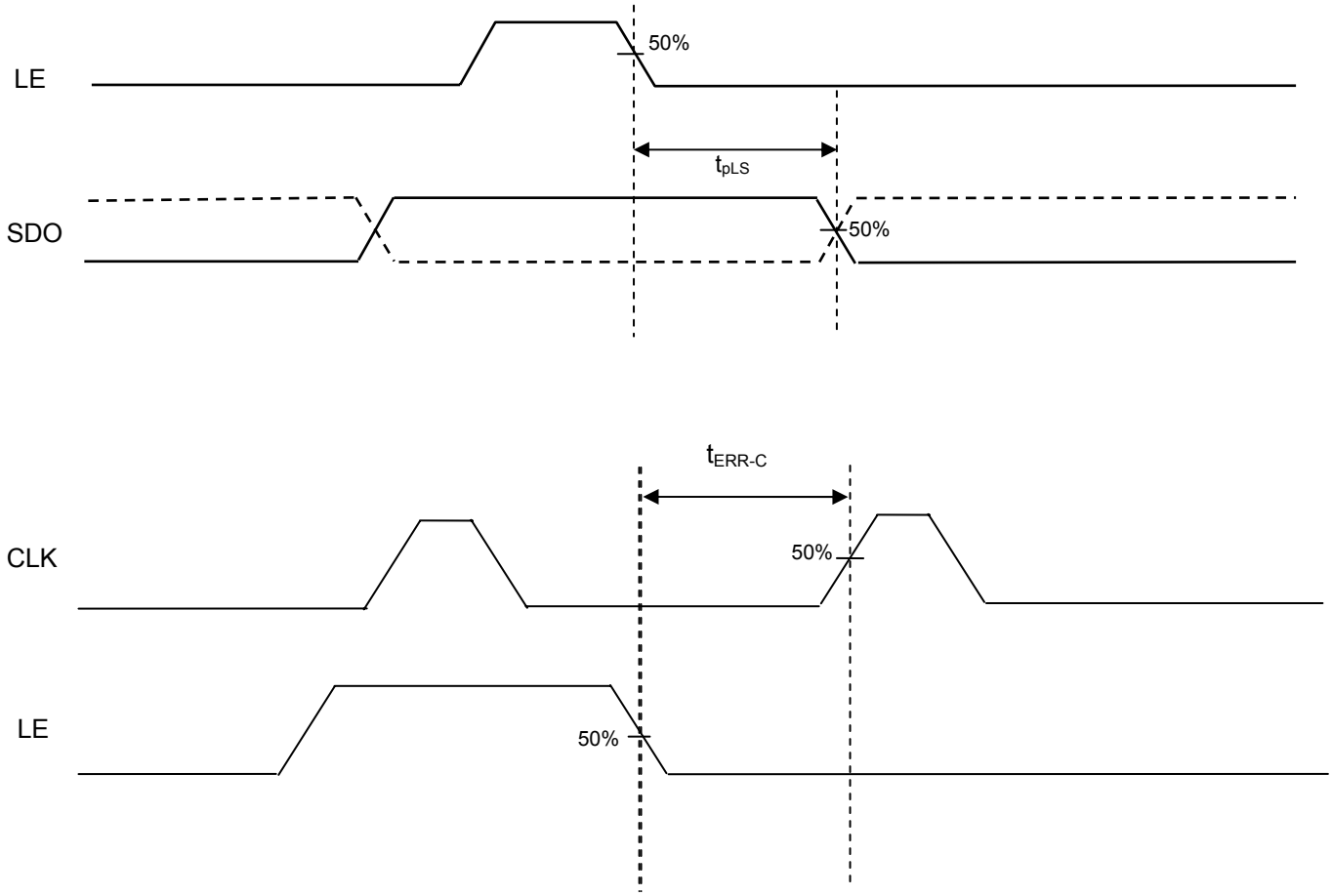
*** $\overline{OE}$ =t_{or}+t_{of}.

Test Circuit for Switching Characteristics



Timing Waveform

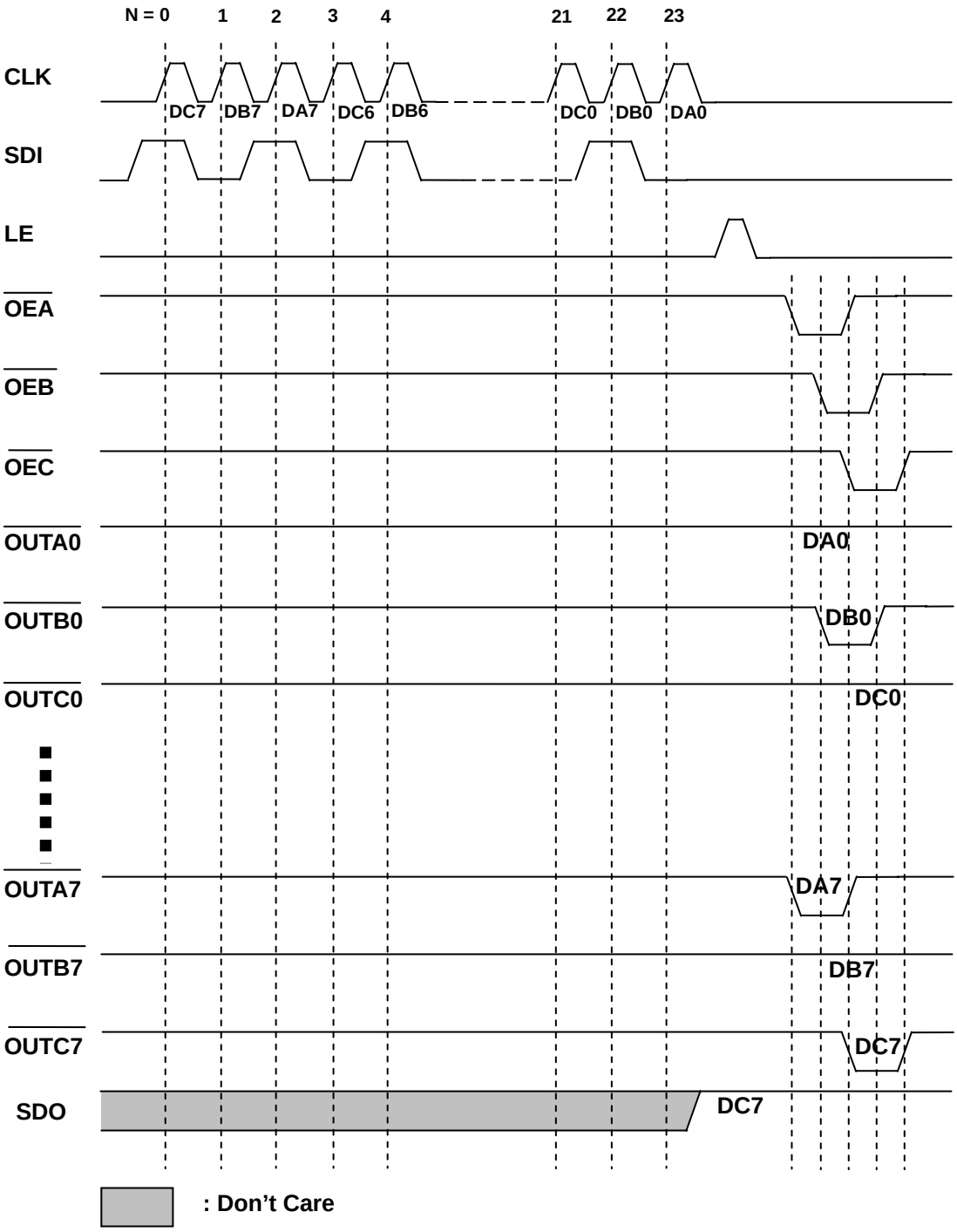



LE
50%
t_{pLS}
SDO
50%
t_{ERR-C}
CLK
50%
LE
50%

Control the Output Ports

The data is shifted from the SDI to the 24-bit shift registers. Both the LE is asserted and no CLK toggles when LE is high, the data in the shift register will be latched to the output latch. This is so-called “series-in parallel- out” mechanism.

When the $\overline{OE}$ is low and the data in the output latch is “1”, the output channel will be turned on and the current will sink into the output port. If LEDs are connected to the output port with adequate power source, the LEDs will be lit up with the preset current.



Control Command

	Signals Combination*	Description
Command Name	**Number of CLK rising edge when LE is asserted**	**Action after a falling edge of LE**
Data latch	0	Latch the serial data to the output latch.
Compulsory open-circuit detection	1	Issue “compulsory open-circuit detection” once. The data latch will not occur.
NA	> 2	No action. SDO shifts out input data from SDI.

*Number of CLK” that not specified above may cause misjudgment of MBI5324. Please refer to the section of “Principle of Operation” for detailed timing diagram.

Data Output From SDO

Command	SDO after a falling edge of LE
Latch Data	Serial data input ; the data has latched into output buffer
Compulsory open-circuit detection	Error code of compulsory open-circuit detection. After the falling edge of LE, it needs to wait t_{ERR-C}*.

*See section of “Principle of Operation” for detailed timing diagram

Error Code

Result	Error flag for corresponding bit in the shift register
Open-circuit error is detected in the channel	0
No open-circuit error is detected in the channel (Or detection is suppressed)	1

If the condition of valid error detection doesn’t match, the detection is suppressed. Please refer to section of “Principle of Operation” for the condition of valid error detection.

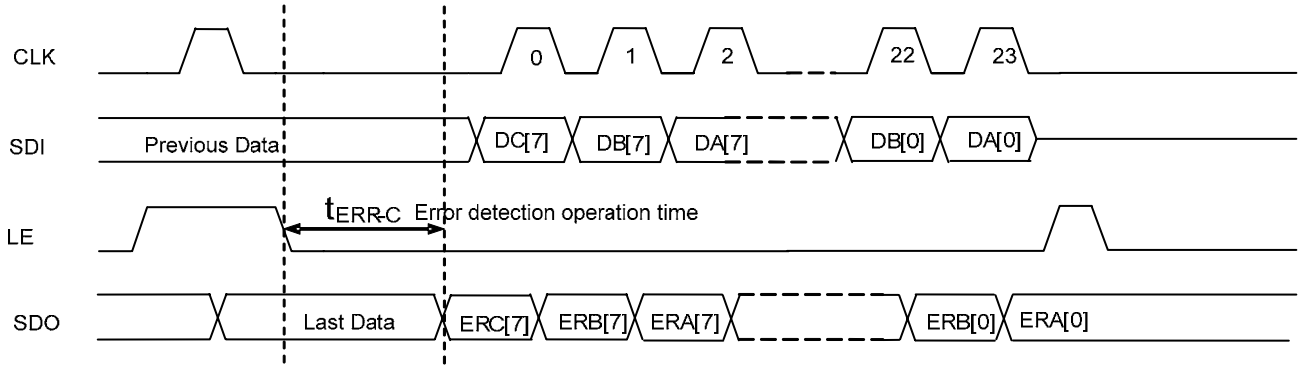
Principle of Operation

Compulsory Open-Circuit Detection

Compulsory open-circuit detection is also named as “silent”, “dark” or “blind” error detection. No matter the data is 1 or 0, the output will be turned on with small current in a short time in the compulsory open-circuit detection mode. The turn-on time and current are short and small, so that the human eye will not perceive detection and the quality of the video and image will not influenced. According to the issued “control commands”, if an LED is open-circuit, the error code will be “0” and shifted out through SDO once only.

The principle of MBI5324 LED compulsory open-circuit detection is based on the fact that the LED loading status is judged by comparing the effective voltage value (V_{DS}) of each output port with the targeted voltage ($V_{OD,TH}$ = 0.3V). Thus, after the command of “compulsory open-circuit detection”, the output ports of MBI5324 will be turned on with small current in a short time. Then, the error status saved in the built-in register will be shifted out through SDO pin bit by bit while receiving the new data simultaneously.

1. Conditions required to activate the compulsory open-circuit detection: (1) falling edge of LE and (2) $\overline{OE}$ =High.
2. Condition of valid error detection: $\overline{OE}$ =high during t_{ERR-C}
3. At the falling edge of LE, all output channels are turned on by small current.
4. The error detection starts and then loads error result to shift register during t_{ERR-C}.
5. If CLK is toggled before t_{ERR-C}, the error detection process will be aborted.

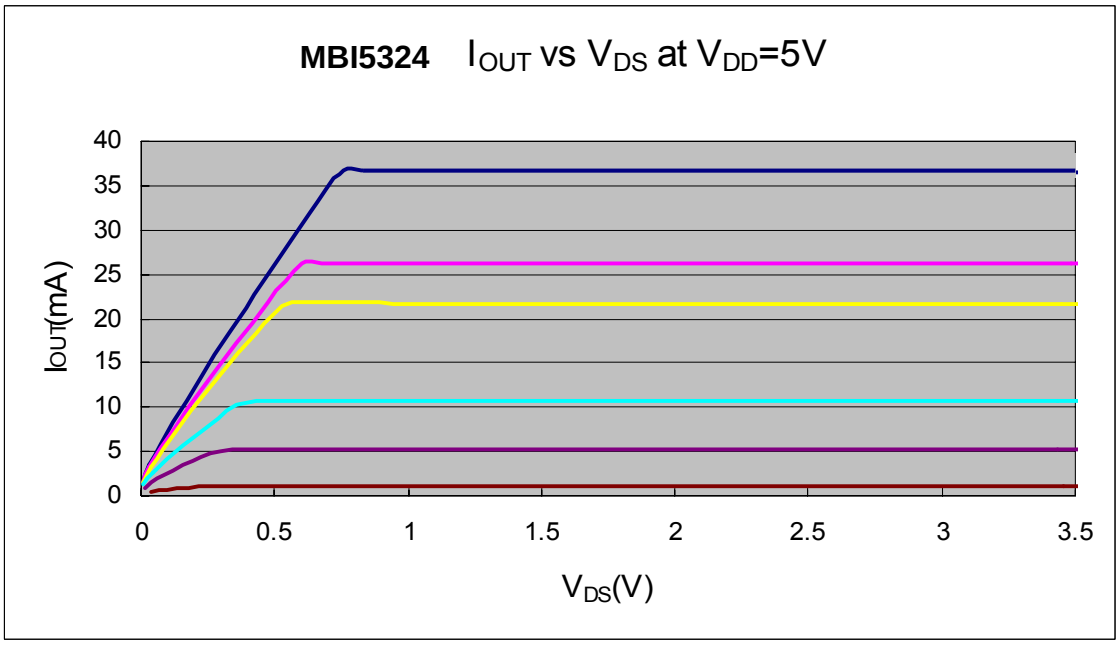


Constant Current

In LED display applications, MBI5324 provides nearly no current variations between channels and ICs. This can be achieved by:

1) While $I_{OUT} \leqq 35mA$, $V_{DD}=5V$, the maximum current skew between different groups from $\overline{OUTA0} \sim \overline{OUTA7}$, $\overline{OUTB0} \sim \overline{OUTB7}$, and $\overline{OUTC0} \sim \overline{OUTC7}$ of channels is less than ±2% (typical), and that of ICs is less than ±4% (typical).

2) In addition, the characteristics curve of output stage in the saturation region is flat and users can refer to the charts as shown below. Thus, the output current keeps constant regardless of the variations of LED forward voltages (V_F). The output current level in the saturation region is defined as output targeted current $I_{out,target}$.



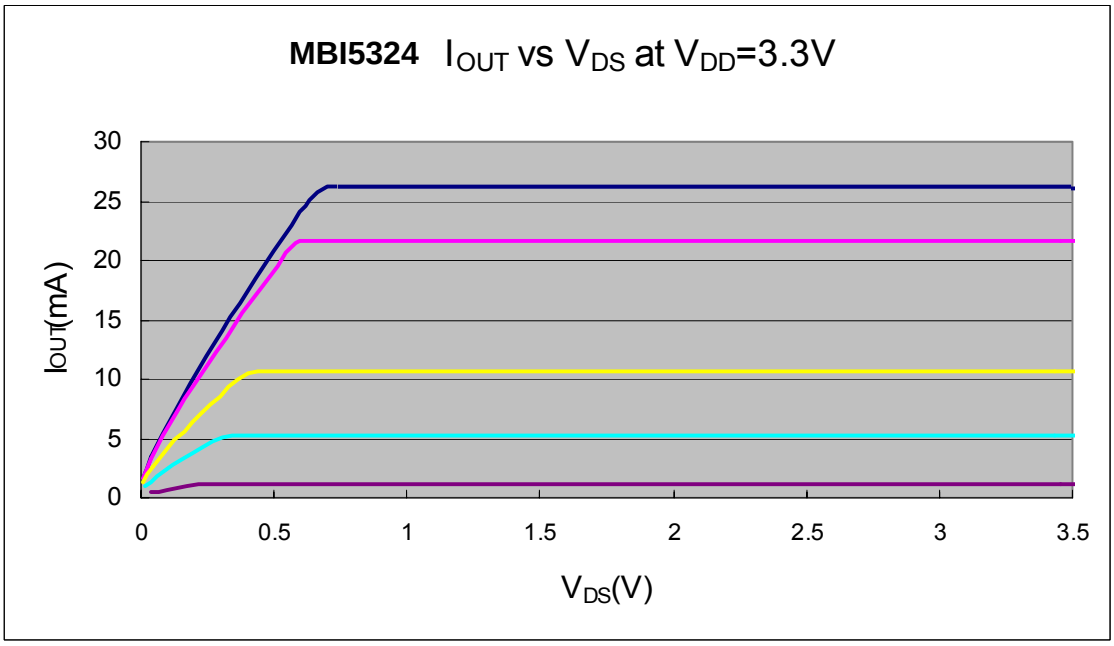


Figure 1

Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

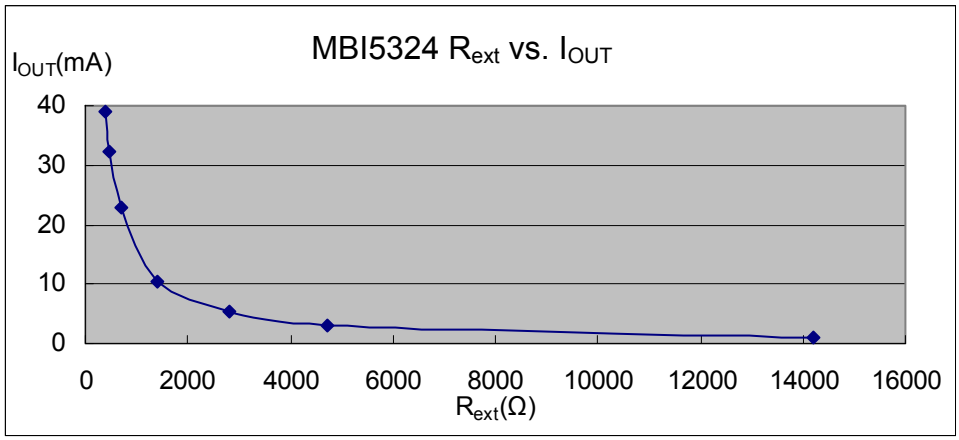


Figure 2

Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=0.62V; I_{OUT}=($V_{R\text{-}EXT}$/R_{ext})x24.0

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. The output current is about 15mA at R_{ext}=1KΩ.

Staggered Delay of Output

MBI5324 has a built-in delayed circuit to perform delayed mechanism. Among output ports exist a graduated t_{stag} delay time(6ns@ V_{DD}=5.0V and 8ns@ V_{DD}=3.3V) among $\overline{OUTAn}$ and $\overline{OUTAn+1}$, $\overline{OUTBn}$ and $\overline{OUTBn+1}$, $\overline{OUTCn}$ and $\overline{OUTCn+1}$ by which the output ports will be turned on at a different time so that the inrush current from the power line will be lowered.

Package Power Dissipation (P_D)

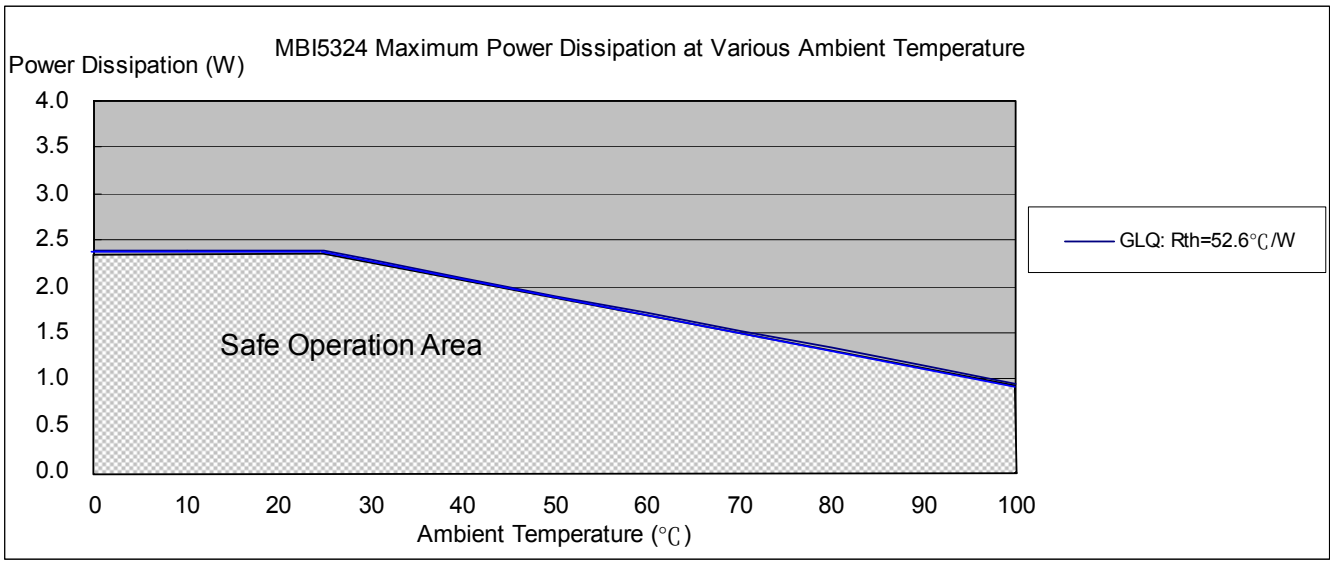
The allowable maximum package heat dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 24 output channels are turned on simultaneously at the same current, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x24)$. Therefore, to keep $P_D(act)\leqq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT} =\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/24$,

where Tj=150°C.

Device Type	$R_{th(j-a)}$ (°C/W)
GLQ	52.6

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.



Load Supply Voltage (V_{LED})

MBI5324 is designed to operate with V_{DS} ranging from 0.4V to 1.0V, considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D(act)}>P_{D(max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer (V_{DROP}).

A voltage reducer lets $V_{DS}= (V_{LED}-V_F)-V_{DROP}$.

Resisters or zener diode can be used in the applications as shown in the following figures.

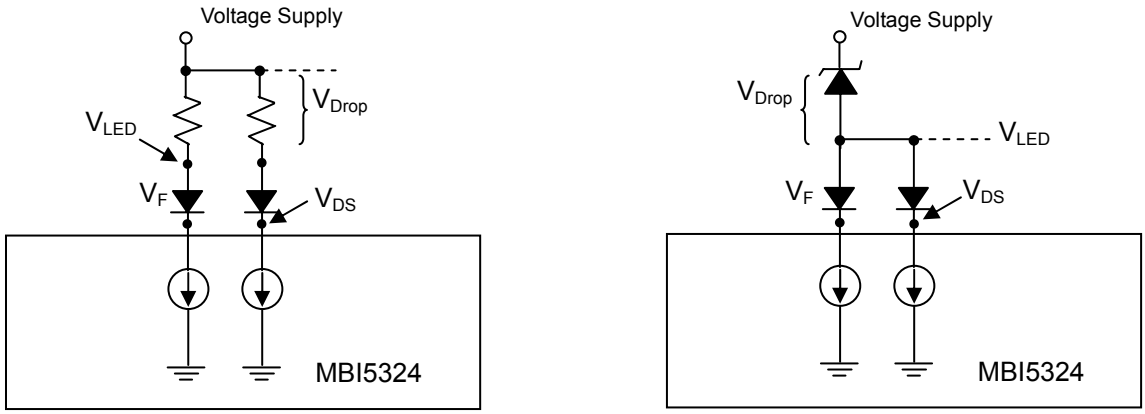


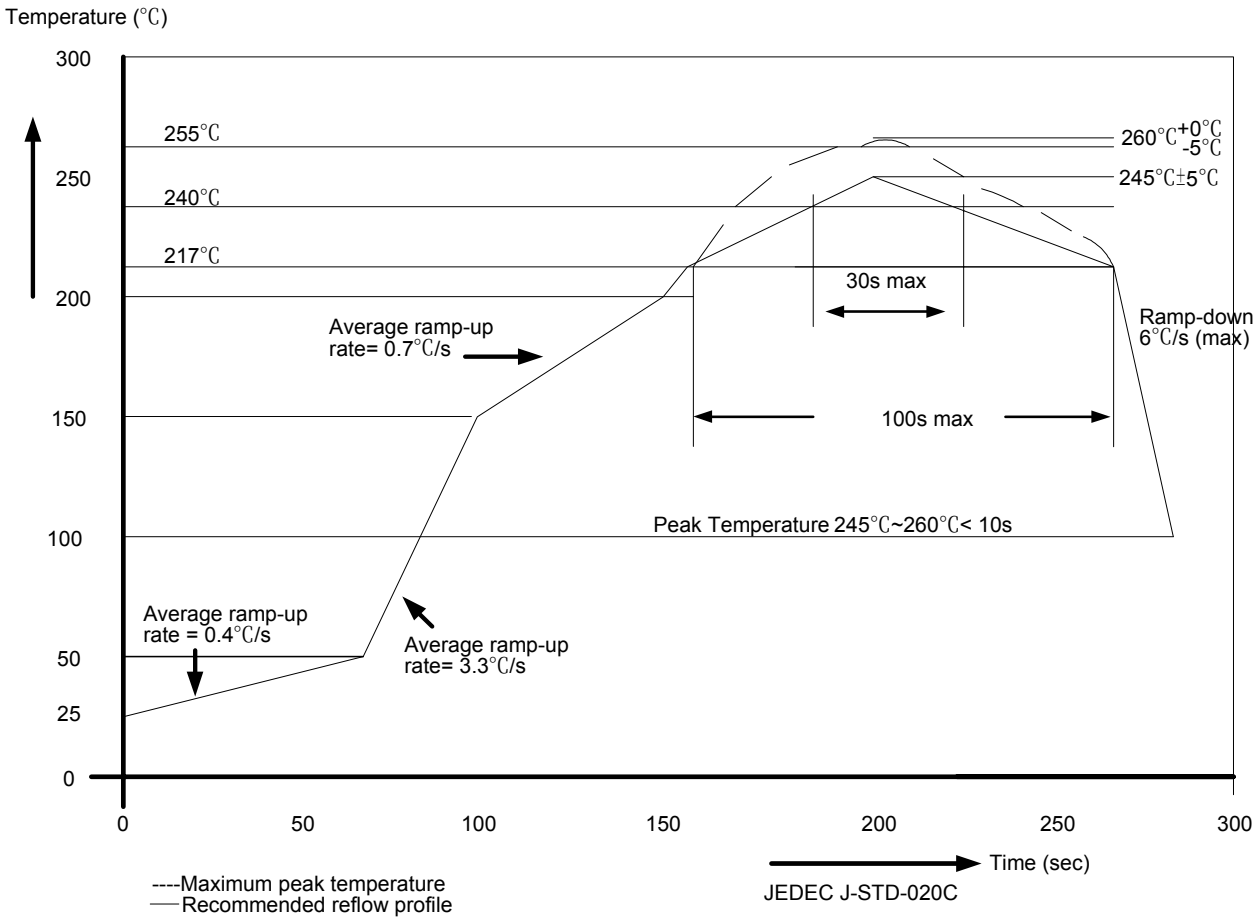
Figure 3

Switching Noise Reduction

LED driver ICs are frequently used in switch-mode applications which always behave with switching noise due to parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Soldering Process of "Pb-free" Package Plating*

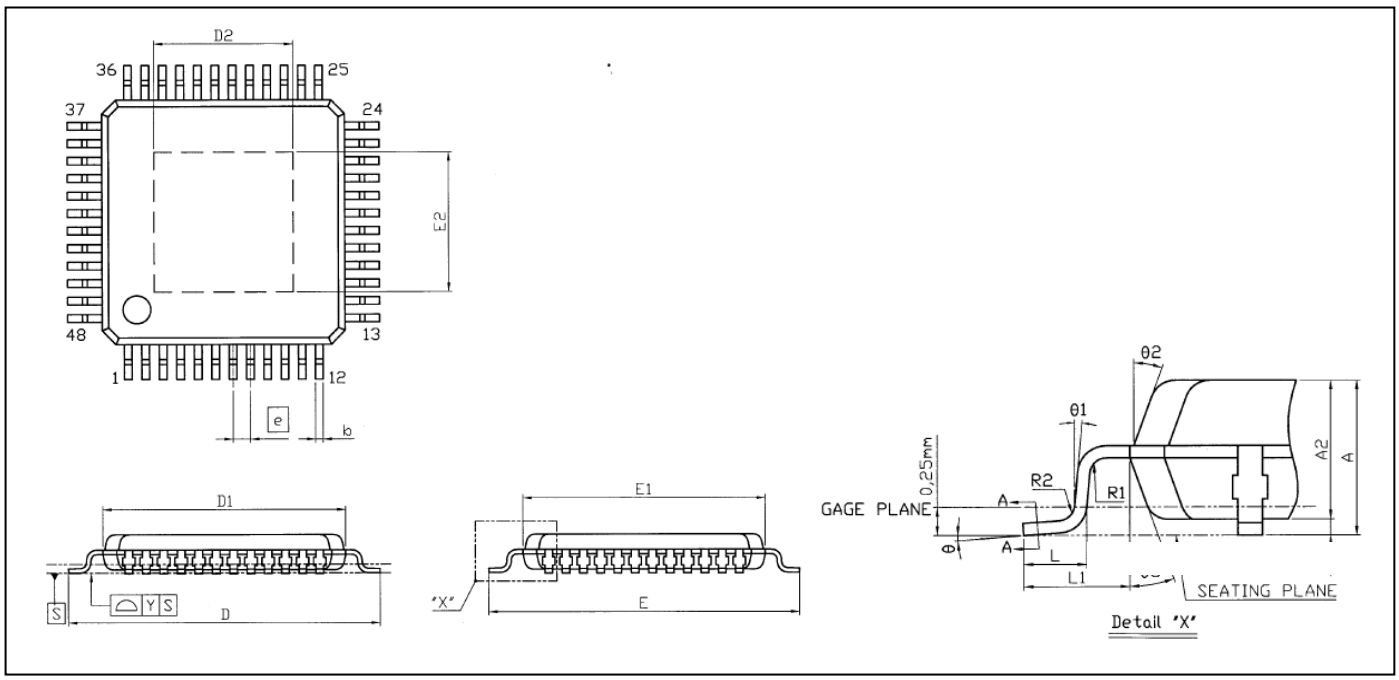
Macroblock has defined "Pb-Free" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to standard 215ºC to 240ºC reflow processes which adopt tin/lead (SnPb) solder paste. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

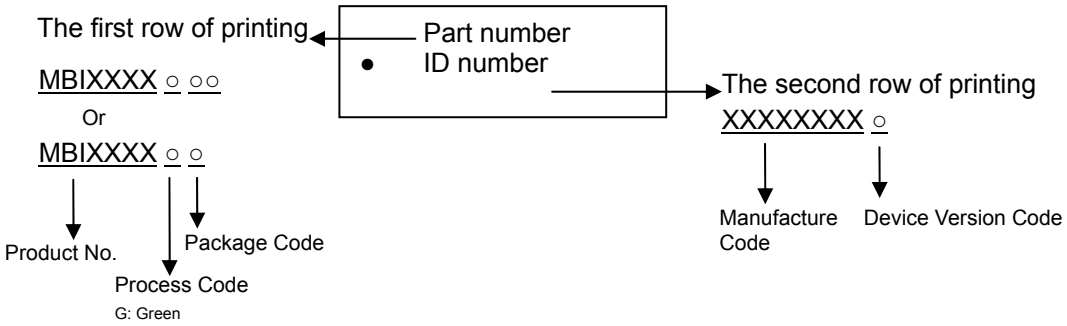
Package Outline



MBI5324GLQ Outline Drawing

Symbol	Dimension (mm)			Dimension (MIL)		
	Min.	Normal	Max.	Min.	Normal	Max.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
D2	4	4.5	5	157	177	197
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
E2	4	4.5	5	157	177	197
e		0.50 BSC			20 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

Product Top-Mark Information



Product Revision History

Datasheet version	Device version code
V1.00	A
V1.00a	A
V1.01	A

Product Ordering Information

Part Number	**"Pb-free & Green" Package Type**	**Weight (g)**
MBI5324GLQ	LQFP48L-7x7-0.5	0.158

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